REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 1-6 and 8-15 are in this application. Claim 1 has been amended. Claim 7 has been cancelled. Claims 8-15 have been added to alternately and additionally claim the present invention.

The Examiner objected to the drawings under 37 CFR 1.83(a) because the drawings do not show an elongated finger configuration. Claim 7, which refers to the elongated finger configuration, has been cancelled.

The Examiner objected to the Abstract of the Disclosure as the Abstract should contain less than 150 words. The Abstract has been amended to be less than 150 words.

The Examiner rejected claims 1-7 under 35 U.S.C. §103(a) as being unpatentable over Oh (U.S. Patent No. 5,986,863). For the reasons set forth below, applicant respectfully traverse this rejection as applied to the amended claims.

Claim 1 recites, in part,

> "a first well region of a second conductivity type disposed in the semiconductor substrate, the first well region having a center region, a side wall surface that contacts the top surface, and a bottom surface that contacts the side wall surface, the bottom surface under the center region contacting the substrate; [and]
> "a first contact region of the first conductivity type disposed in the center region of the first well region and spaced apart from the first floating region." [Brackets added.]

In rejecting the claims, the Examiner pointed to substrate 10 shown in FIG. 4 of Oh as constituting the substrate of claim 1, and n-well region 30 shown in FIG. 4 of Oh as constituting the first well region of claim 1. The Examiner also pointed to p-type region 32 shown in FIG. 4 of Oh, which is formed in the center region of n-well 30, as constituting the first contact region of claim 1.

The Oh reference, however, fails to teach or suggest that the bottom surface of the first well region under the center region contacts the substrate. As shown in FIG. 4, Oh teaches that the bottom surface of n-well 30 that underlies p+ region 32 (and n+ region 34) contacts second buried region 14. Thus, since Oh does not teach or suggest that the bottom

surface of the first well region under the center region contacts the substrate, claims 1-6 are patentable over the Oh reference.

New claim 8 recites, in part,

> "a first contact region of the first conductivity type formed in the first well, the first contact region being electrically connected to a first node;
> "a second contact region of the second conductivity type formed in the first well, the second contact region being electrically connected to the first node."

However, if n-well 30 is read to be the first well of claim 8, p+ region 32 is read to be the first contact region, and n+ region 34 is read to be the second contact region, then the Oh reference fails to teach or suggest that p+ region 32 and n+ region 34 are electrically connected to the same node. As shown in FIG. 4 of Oh, p+ region 32 is connected to a node that is connected to n+ region 24, while n+ region 34 is connected to node Vcc2. Thus, since Oh does not teach or suggest that the first and second contact regions are electrically connected to the same node, claims 8-15 are patentable over the Oh reference.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

PILLSBURY WINTHROP LLP

Dated: 3-5-02 By: _____

Mark C. Pickering
Registration No. 36,239

Attorney for Assignee

50 Fremont Street, Fifth Floor
San Francisco, CA 94105-2228
Direct Dial Telephone No. (415) 983-1297
Telephone: (415) 983-1000
Facsimile: (415) 983-1200

APPENDIX

In the Abstract

Please amend the Abstract as follows:

An ESD protection structure [for use with ICs that can protect from ESD events of both positive and negative polarities, has a low snapback holding voltage and a high maximum snapback current. The ESD protection structure] includes a semiconductor substrate of a first conductivity type [(typically P-type)], and first and second well regions of a second conductivity type [(typically N-type),] disposed in the substrate. The first and second well regions are separated by a gap region of [the first conductivity type in] the substrate. Also included are first and second floating regions (of the second conductivity type) disposed in the first and second well regions adjacent to the gap region, respectively. The ESD protection structure also includes first and second contact regions of the first conductivity type disposed on the first and second well regions, respectively, and spaced apart from the first and second floating regions, respectively. The ESD protection structure also includes first and second contact regions of the second conductivity type disposed on the first and second well regions, respectively, and spaced apart from the first and second floating regions, respectively. [During operation, the ESD protection structure undergoes primary breakdown by low current avalanche breakdown of the gap region between the first and second floating regions, followed by "double injection" of both holes and electrons, thereby providing for a low snapback holding voltage and a high maximum snapback current. The symmetrical nature of the ESD protection structure provides for protection from both positive and negative ESD events.]

Please amend claim 1 as follows:

1. (Amended) An ESD protection structure for use with an integrated circuit comprising:

a semiconductor substrate of a first conductivity type having a top surface;

a first well region of a second conductivity type disposed in the semiconductor substrate, the first well region having a center region, a side wall surface that contacts the top surface, and a bottom surface that contacts the side wall surface, the bottom surface under the center region contacting the substrate;

a second well region of the second conductivity type disposed in the semiconductor substrate;

a gap region of the first conductivity type disposed in the semiconductor substrate and separating the first well region from the second well region,

a first floating region of the second conductivity type disposed in the first well region adjacent to the gap region;

a second floating region of the second conductivity type disposed in the second well region adjacent to the gap region;

a first contact region of the first conductivity type disposed [on] in the center region of the first well region and spaced apart from the first floating region;

a second contact region of the first conductivity type disposed [on] in the second well region and spaced apart from the second floating region;

a first contact region of the second conductivity type disposed [on] in the center region of the first well region and spaced apart from the first floating region; and

a second contact region of the second conductivity type disposed [on] in the second well region and spaced apart from the second floating region.

Claims 8-15 have been added.